

Features

- Center amplifying gate
- Metal case with ceramic insulator
- Low on-state and switching losses

Typical Applications

- AC controllers
- DC and AC motor control
- Controlled rectifiers

$I_{T(AV)}$ **1070A**
 V_{DRM}/V_{RRM} **1100~1800V**
 I_{TSM} **12 kA**
 I^2t **720 10³A²S**



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _j (°C)	VALUE			UNIT
				Min	Type	Max	
I _{T(AV)}	Mean on-state current	180° half sine wave 50Hz Double side cooled,	T _C =55°C			1260	A
			T _C =70°C			1070	
V _{DRM} V _{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V _{DRM} &V _{RRM} tp=10ms V _{DSM} &V _{RSM} = V _{DRM} &V _{RRM} +100V	125	1100		1800	V
I _{DRM} I _{RRM}	Repetitive peak current	V _{DM} = V _{DRM} V _{RM} = V _{RRM}	125			50	mA
I _{TSM}	Surge on-state current	10ms half sine wave	125			12	kA
I ² t	I ² T for fusing coordination	V _R =0.6V _{RRM}				720	A ² s*10 ³
V _{TO}	Threshold voltage		125			0.91	V
r _T	On-state slop resistance					0.35	mΩ
V _{TM}	Peak on-state voltage	I _{TM} =2400A, F= 18kN	125			1.75	V
dv/dt	Critical rate of rise of off-state voltage	V _{DM} =0.67V _{DRM}	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	V _{DM} = 67%V _{DRM} to 1500A, Gate pulse t _r ≤0.5μs I _{GM} =1.5A	125			100	A/μs
Q _{rr}	Recovery charge	I _{TM} =2000A, tp=1000μs, di/dt=-20A/μs, V _R =50V	125		1200		μC
I _{GT}	Gate trigger current	V _A =12V, I _A =1A	25	40		300	mA
V _{GT}	Gate trigger voltage			0.8		3.0	V
I _H	Holding current			20		250	mA
V _{GD}	Non-trigger gate voltage	V _{DM} =0.67V _{DRM}	125	0.3			V
R _{th(j-c)}	Thermal resistance Junction to case	At 180° sine double side cooled Clamping force 18kN				0.028	°C /W
R _{th(c-h)}	Thermal resistance case to heatsink					0.0075	
F _m	Mounting force			15		20	kN
T _{stg}	Stored temperature			-40		140	°C
W _t	Weight					320	g
Outline	KT39cT40						

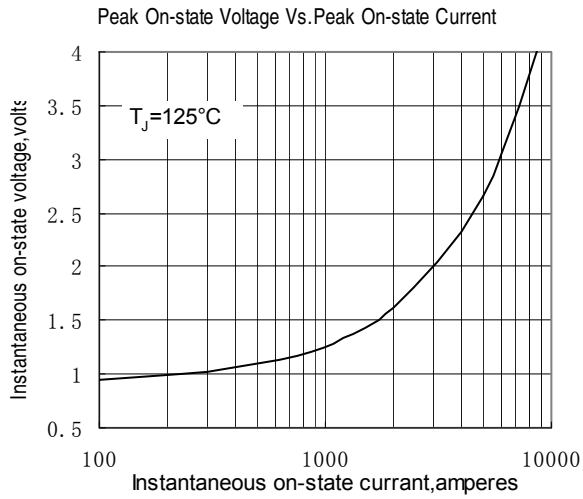


Fig.1

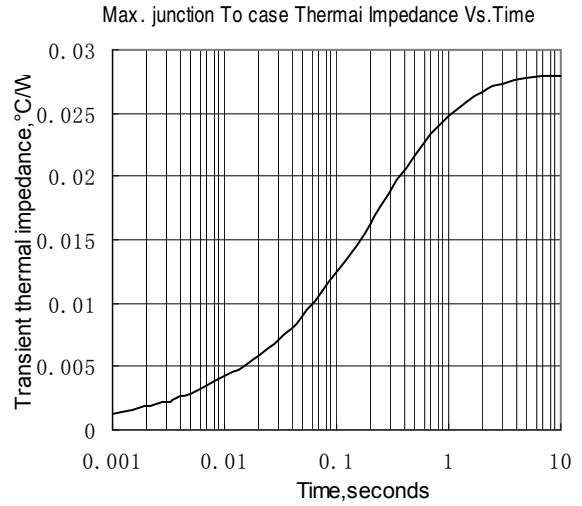


Fig.2

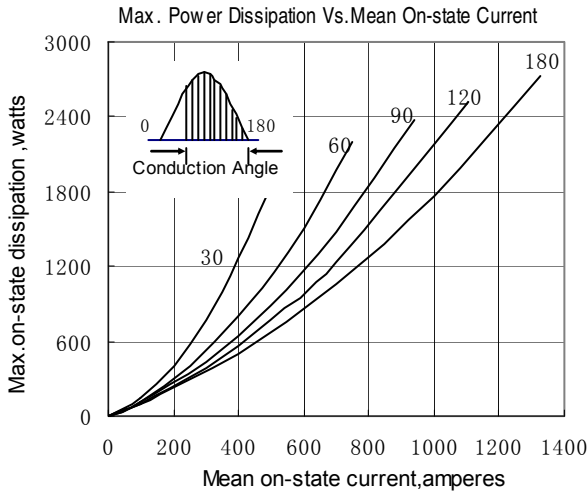


Fig.3

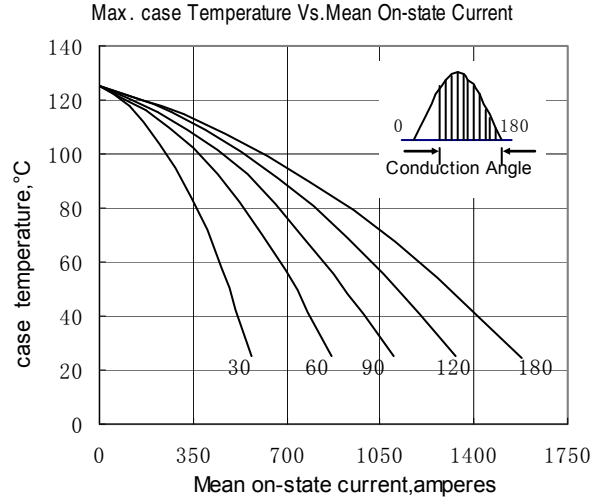


Fig.4

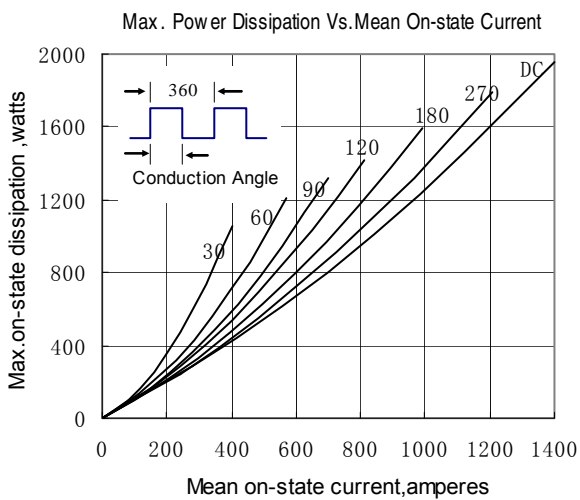


Fig.5

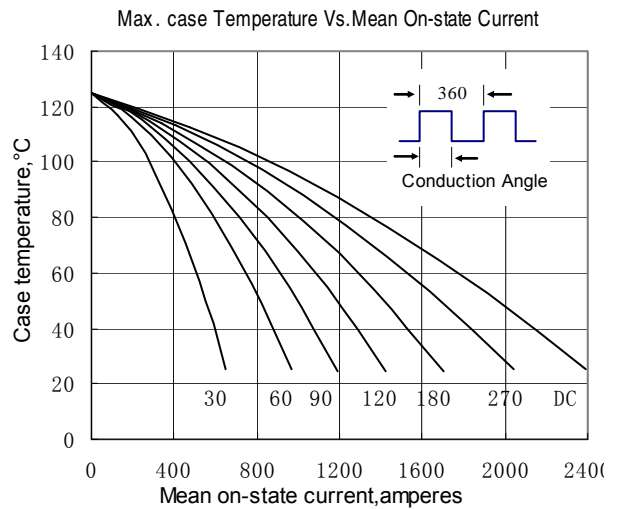


Fig.6

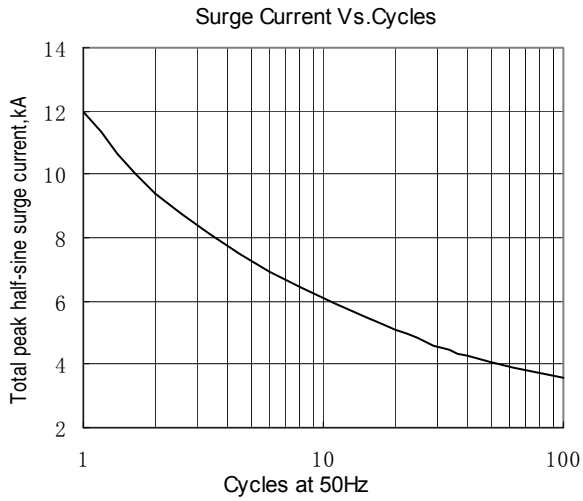


Fig.7

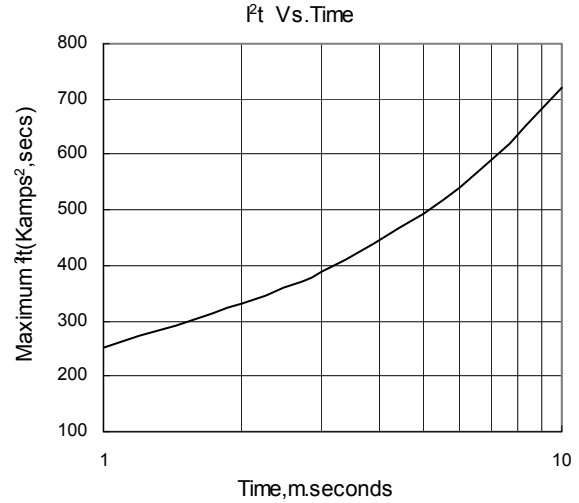


Fig.8

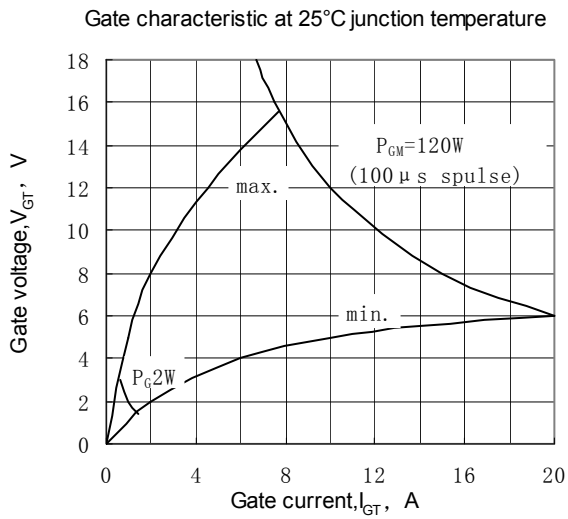


Fig.9

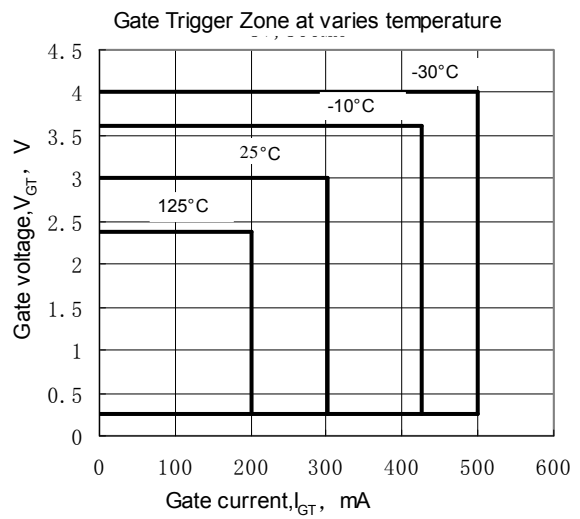


Fig.10

Outline:

